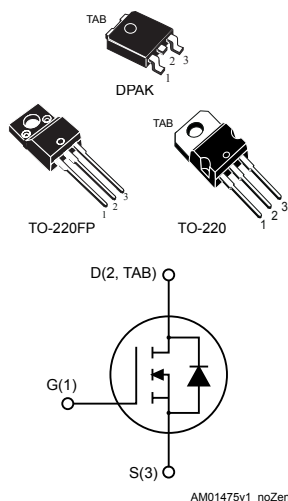


N-channel 250 V, 0.140 Ω typ., 17 A STripFET™ II Power MOSFETs in DPAK, TO-220FP and TO-220 packages



Features

Order code	V_{DS}	$R_{DS(on)max.}$	I_D	P_{TOT}
STD17NF25	250 V	0.165 Ω	17 A	90 W
STF17NF25				25 W
STP17NF25				90 W

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link

[STD17NF25](#)
[STF17NF25](#)
[STP17NF25](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, DPAK	TO-220FP	
V_{DS}	Drain-source voltage	250		V
V_{GS}	Gate-source voltage	± 20		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	17	17 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	10	10 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	68	68 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	90	25	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	10		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)		2.5	kV
T_j	Operating junction temperature range	-55 to 150		$^{\circ}\text{C}$
T_{stg}	Storage temperature range			

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	TO-220	
R _{thj-case}	Thermal resistance junction-case	1.38	5	1.38	°C/W
R _{thj-amb}	Thermal resistance junction-ambient		62.5		
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	50			

1. When mounted on 1inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	17	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	100	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	250			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 250\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 250\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			10	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 8.5\text{ A}$		0.140	0.165	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1000	-	μF
C_{oss}	Output capacitance			178		
C_{rss}	Reverse transfer capacitance			28		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }200\text{ V}$, $V_{GS} = 0\text{ V}$	-	135	-	μF
R_g	Gate input resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	2	-	Ω
Q_g	Total gate charge	$V_{DD} = 200\text{ V}$, $I_D = 17\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	29.5	-	nC
Q_{gs}	Gate-source charge			4.8		
Q_{gd}	Gate-drain charge			15.6		

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 125\text{ V}$, $I_D = 8.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	8.8	-	ns
t_r	Rise time			17.2		
$t_{d(off)}$	Turn-off delay time			21		
t_f	Fall time			8.8		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				68	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	157		ns
Q_{rr}	Reverse recovery charge			0.91		μC
I_{RRM}	Reverse recovery current			11.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	196		ns
Q_{rr}	Reverse recovery charge			1.34		μC
I_{RRM}	Reverse recovery current			13.7		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

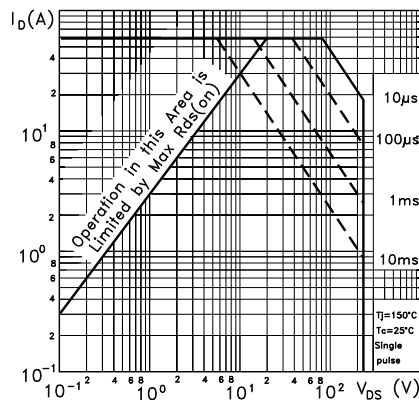
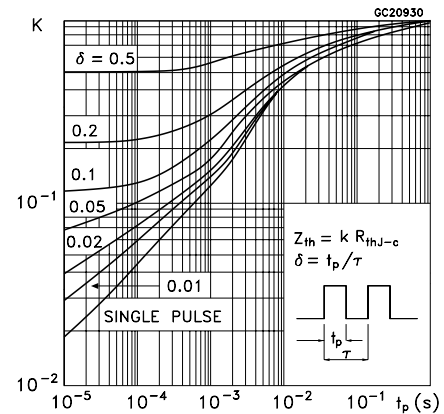
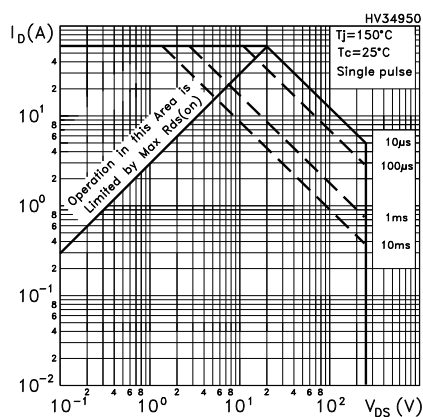
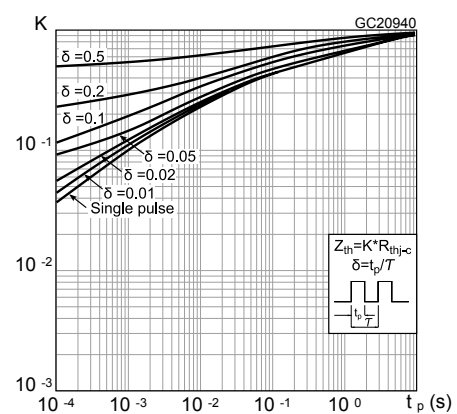
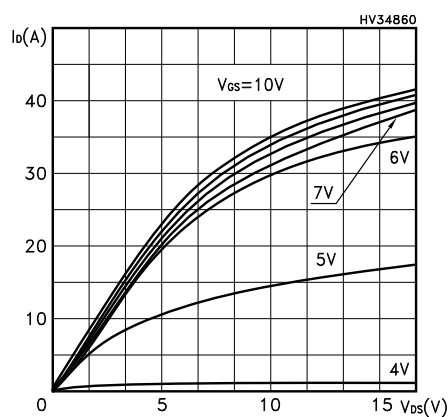
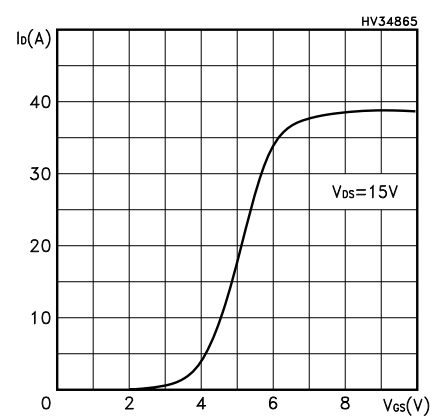
Figure 1. Safe operating area for DPAK, TO-220

Figure 2. Thermal impedance for DPAK, TO-220

Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

Figure 5. Output characteristics

Figure 6. Transfer characteristics


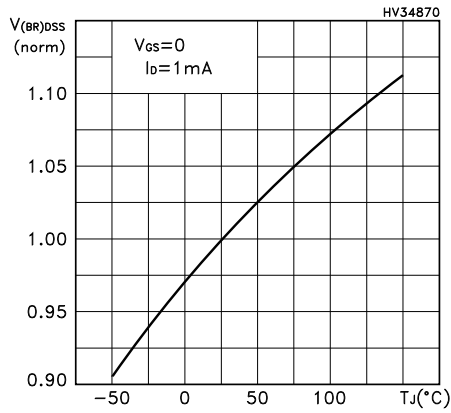
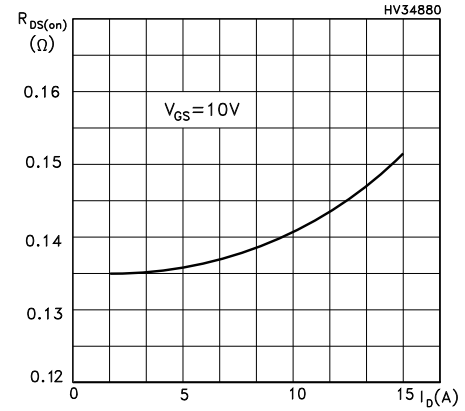
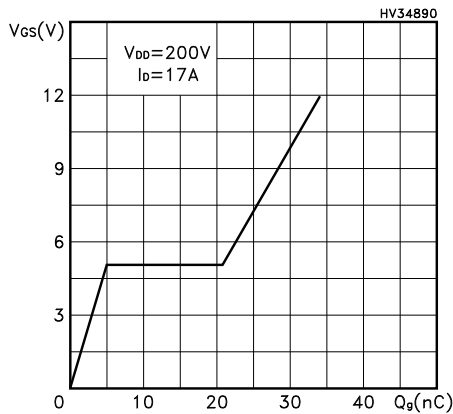
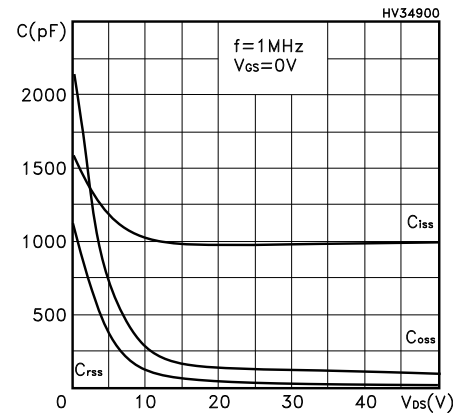
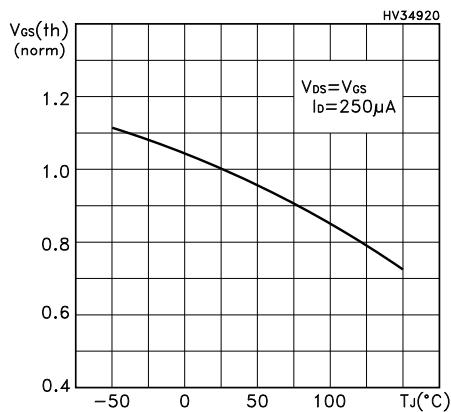
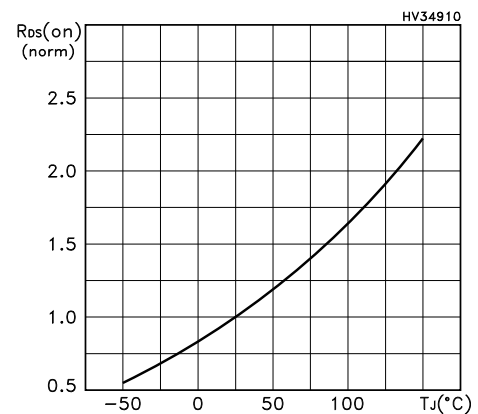
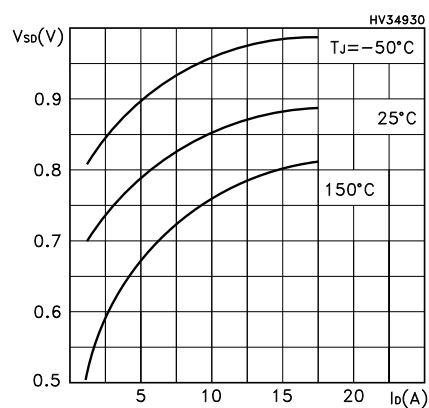
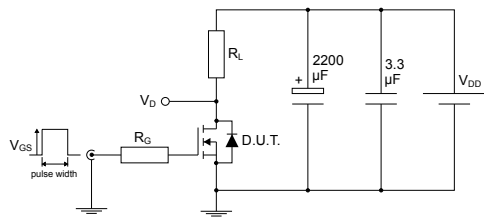
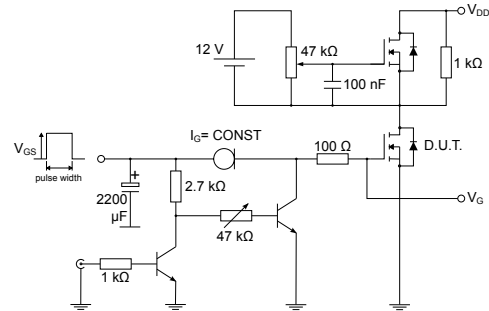
Figure 7. Normalized $V_{(BR)DSS}$ vs temperature

Figure 8. Static drain-source on resistance

Figure 9. Gate charge vs gate-source voltage

Figure 10. Capacitance variations

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on resistance vs temperature


Figure 13. Source-drain diode forward characteristics


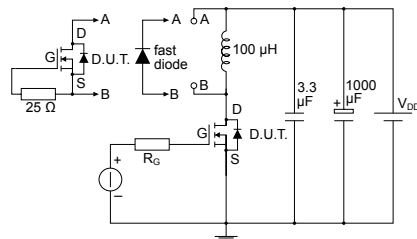
3 Test circuits

Figure 14. Test circuit for resistive load switching times


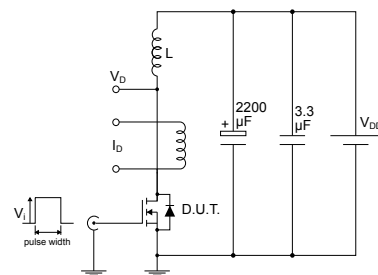
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Figure 15. Test circuit for gate charge behavior


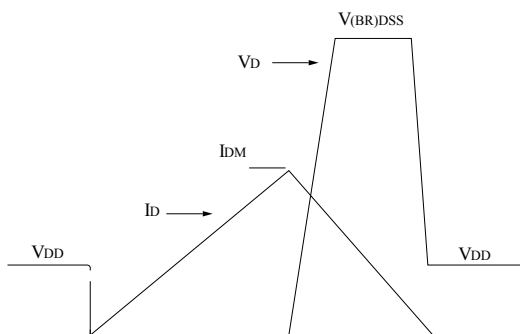
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Figure 16. Test circuit for inductive load switching and diode recovery times


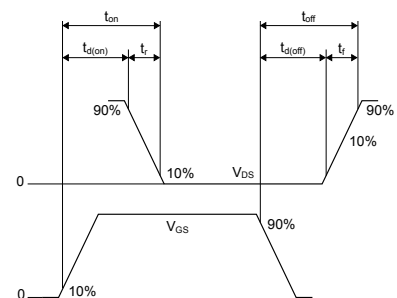
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Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


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Figure 19. Switching time waveform


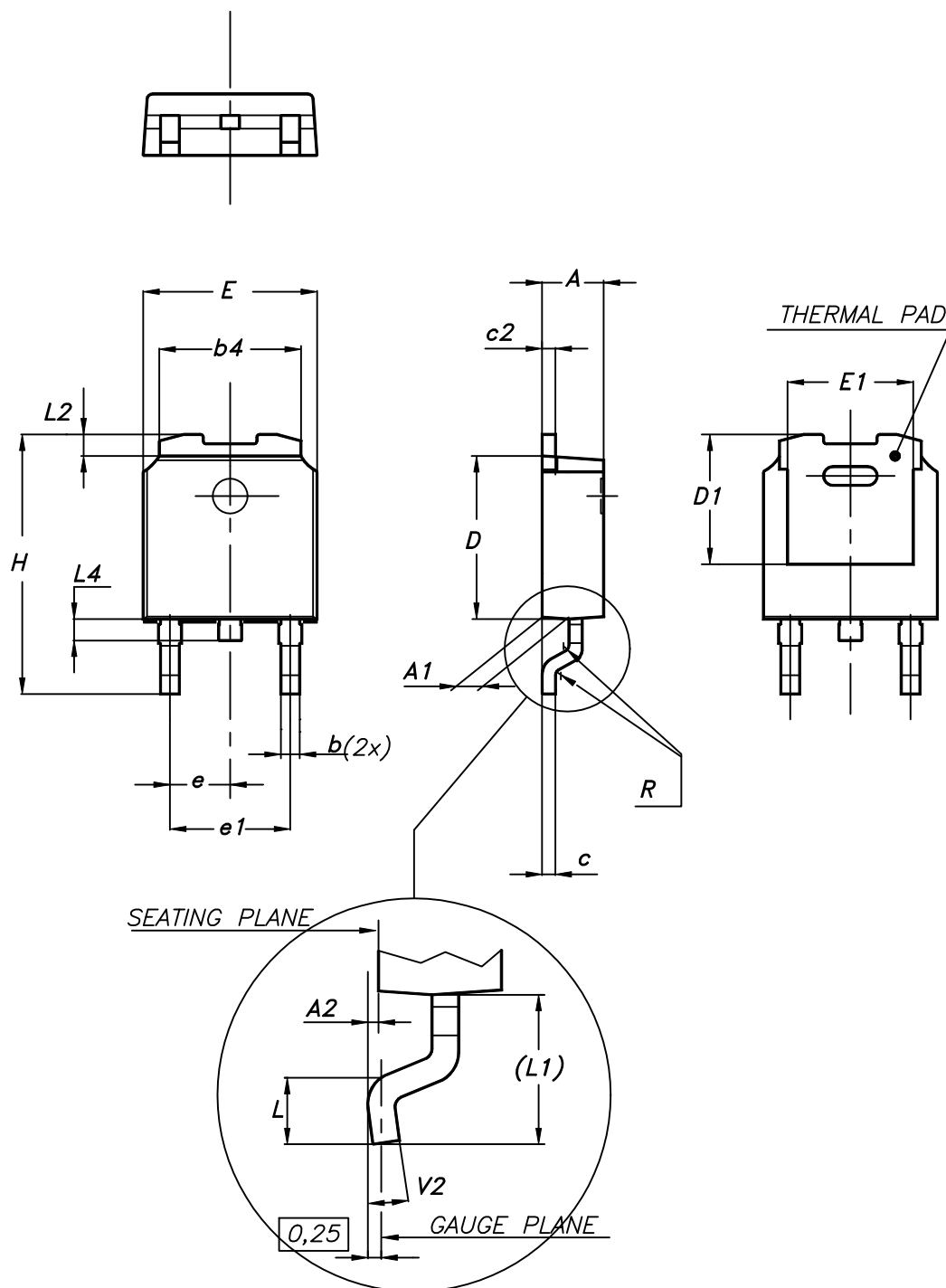
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 20. DPAK (TO-252) type A2 package outline



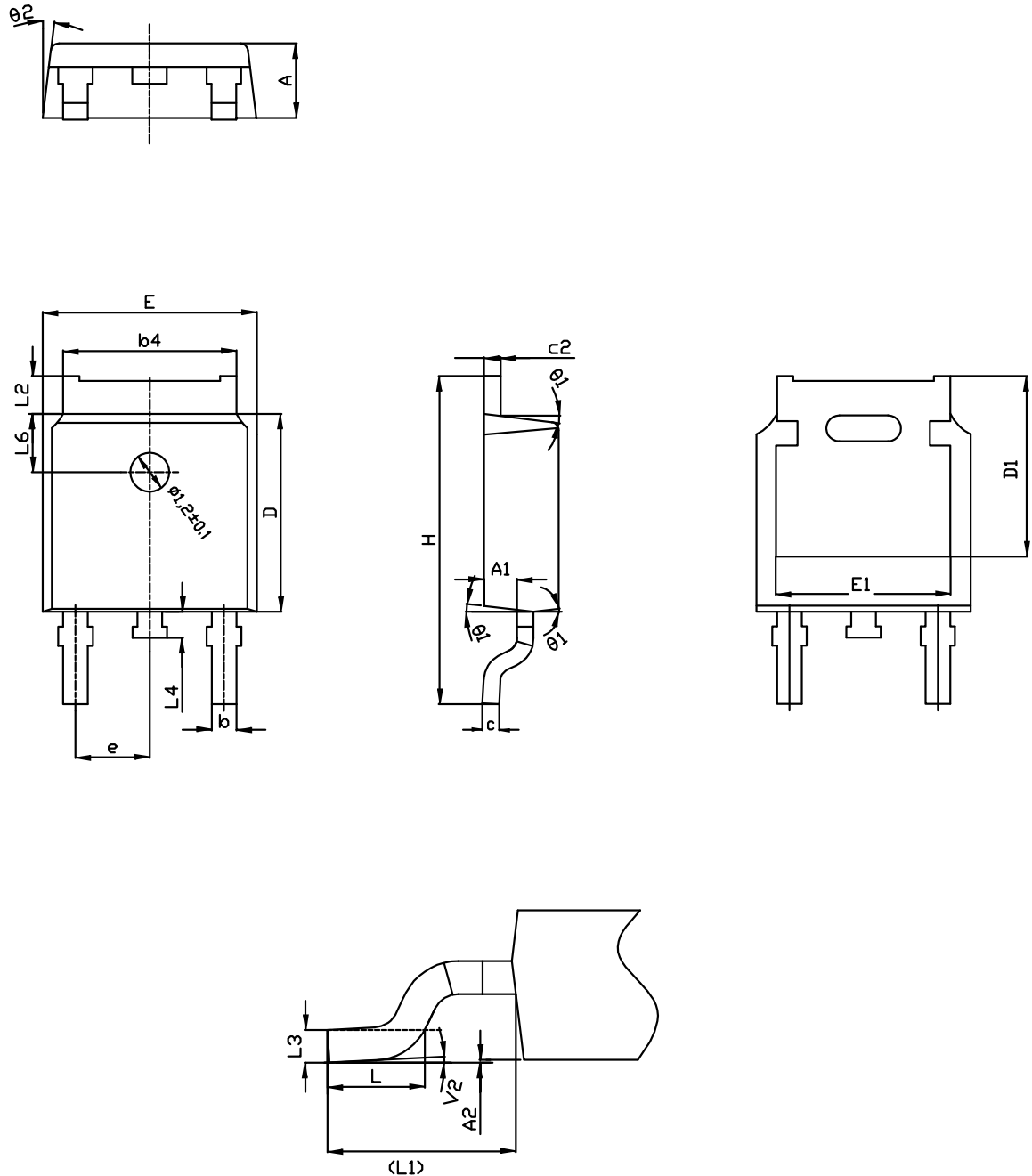
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Table 8. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

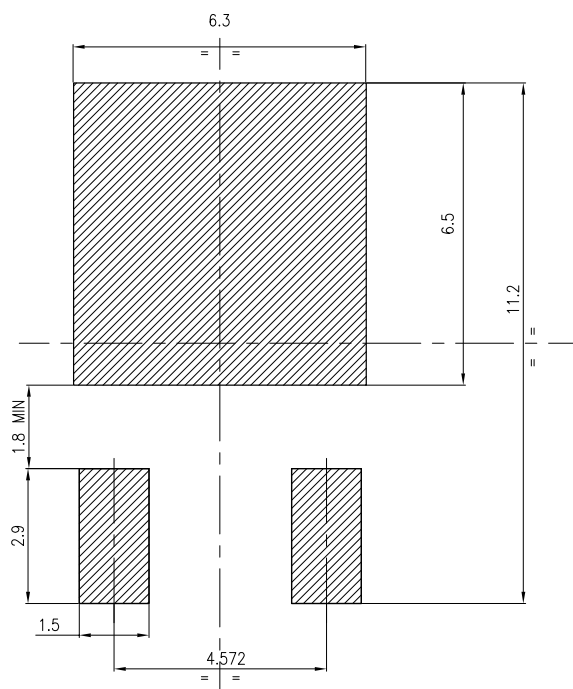
Figure 21. DPAK (TO-252) type C2 package outline



0068772_C2_25

Table 9. DPAK (TO-252) type C2 mechanical data

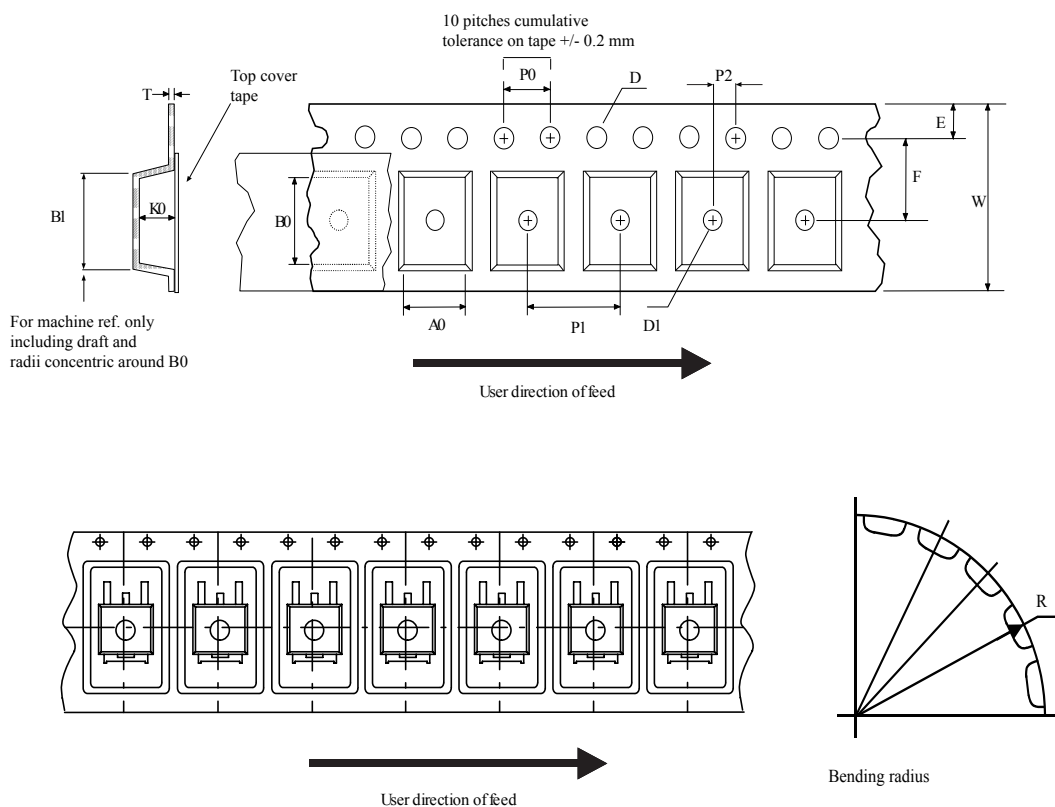
Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 22. DPAK (TO-252) recommended footprint (dimensions are in mm)


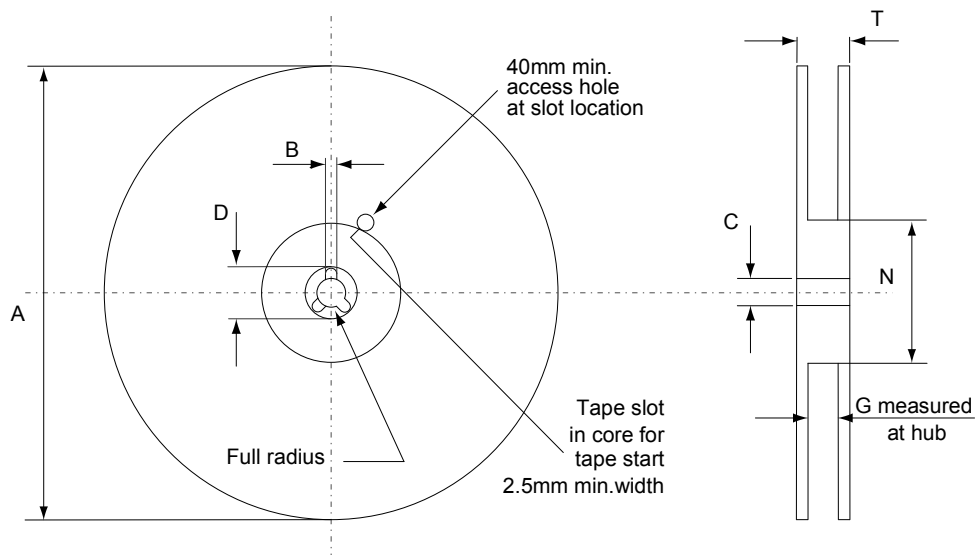
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4.3 DPAK (TO-252) packing information

Figure 23. DPAK (TO-252) tape outline



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Figure 24. DPAK (TO-252) reel outline


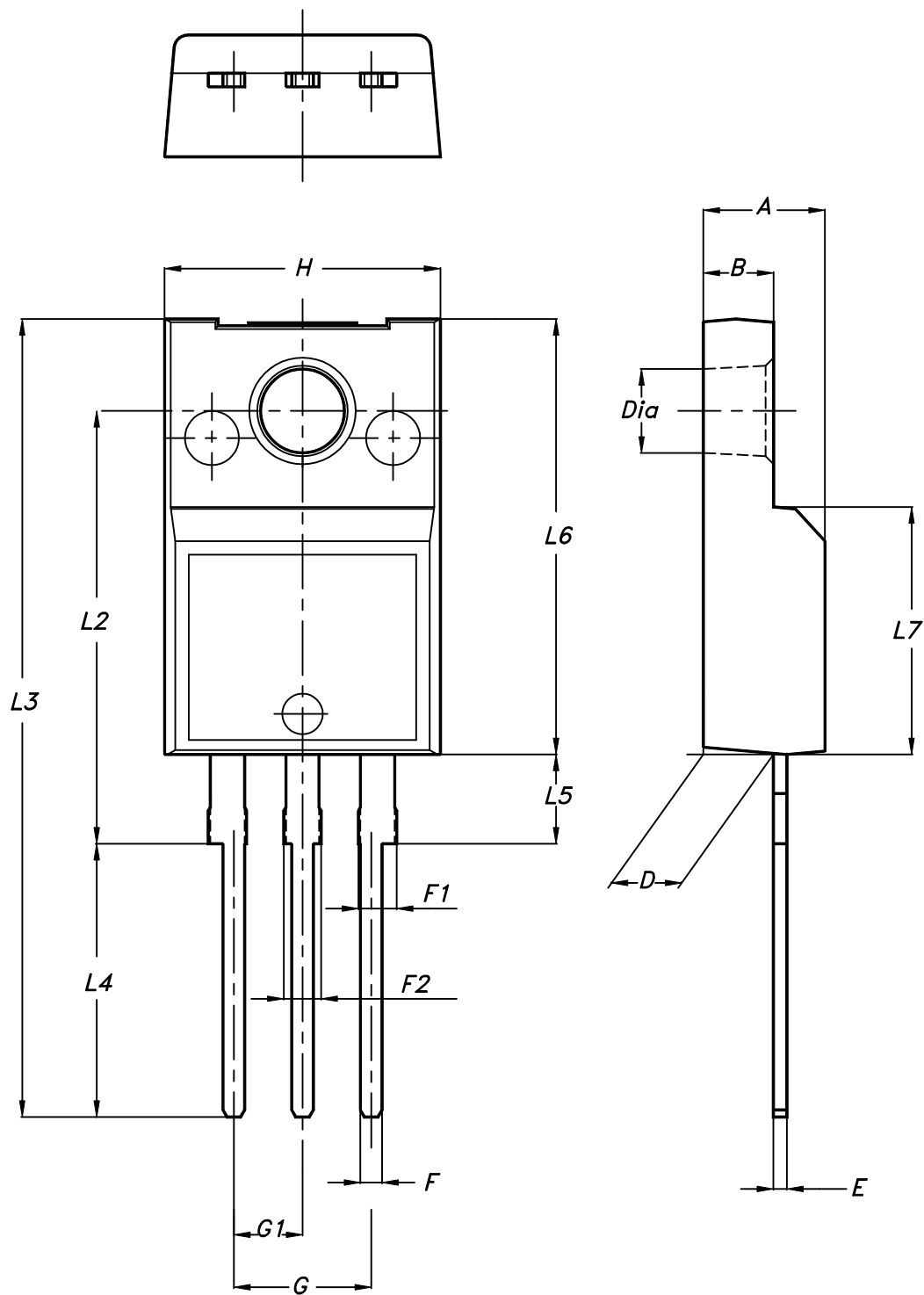
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Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220FP package information

Figure 25. TO-220FP package outline



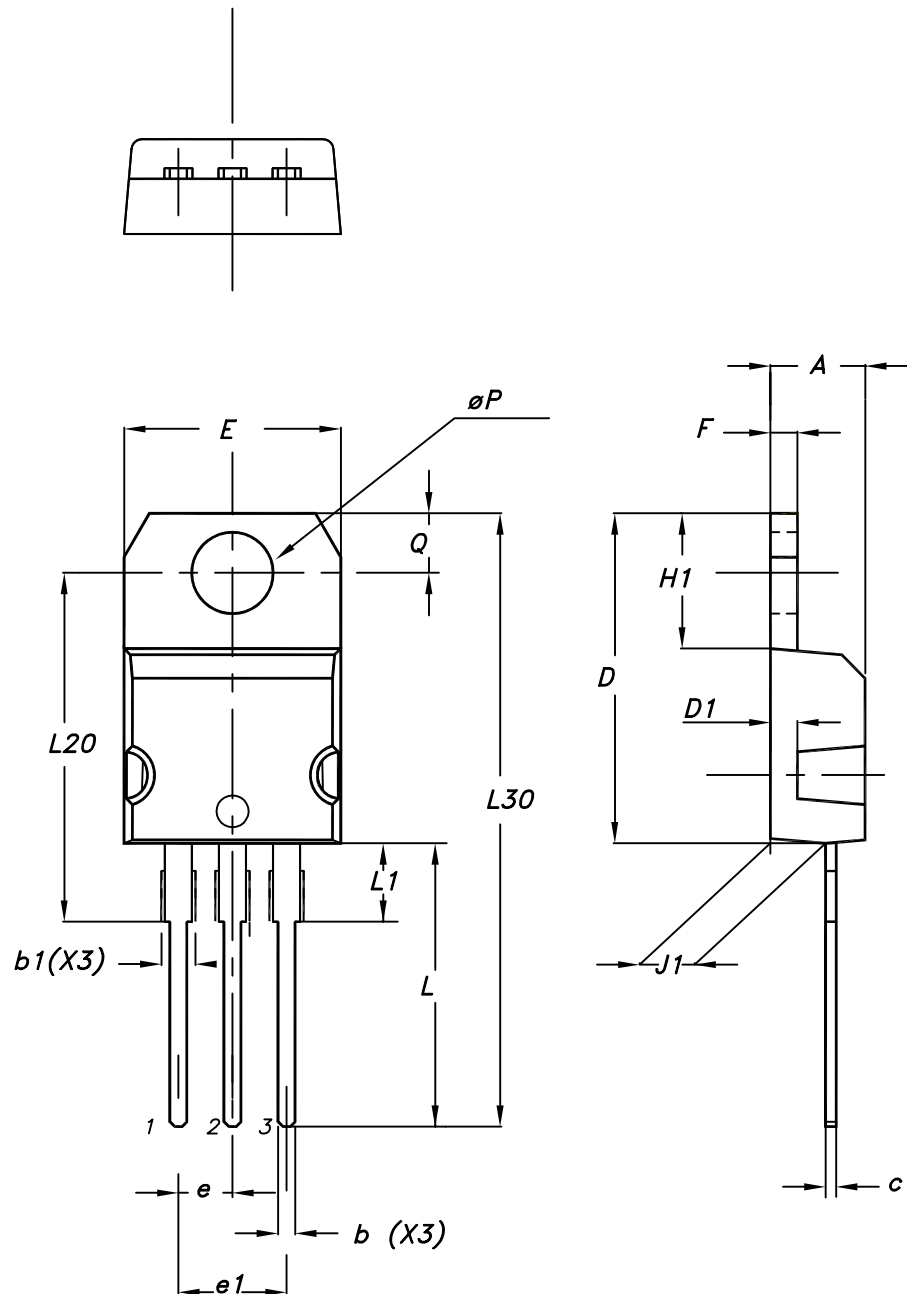
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Table 11. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.5 TO-220 type A package information

Figure 26. TO-220 type A package outline



0015988_typeA_Rev_21

Table 12. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Ordering information

Table 13. Order codes

Order code	Marking	Package	Packing
STD17NF25	17NF25	DPAK	Tape and reel
STF17NF25		TO-220FP	Tube
STP17NF25		TO-220	

Revision history

Table 14. Document revision history

Date	Version	Changes
01-Feb-2007	1	First release.
07-Nov-2012	2	Minor text changes. The part number ST117NF25 has been moved to a separate datasheet. <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i> have been updated.
28-May-2018	3	Removed maturity status indication from cover page. The document status is production data. Updated title in cover page, Section 1 Electrical ratings , Section 2 Electrical characteristics and Section 4 Package information . Minor text changes

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