



STB80PF55 STP80PF55

P-channel 55 V, 0.016 Ω , 80 A TO-220, D²PAK
STripFET™ II Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STP80PF55	55V	<0.018 Ω	80A
STB80PF55	55V	<0.018 Ω	80A

- Extremely dv/dt capability
- 100% avalanche tested
- Application oriented characterization

Application

- Switching applications

Description

These Power MOSFETs are the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps allowing remarkable manufacturing reproducibility.

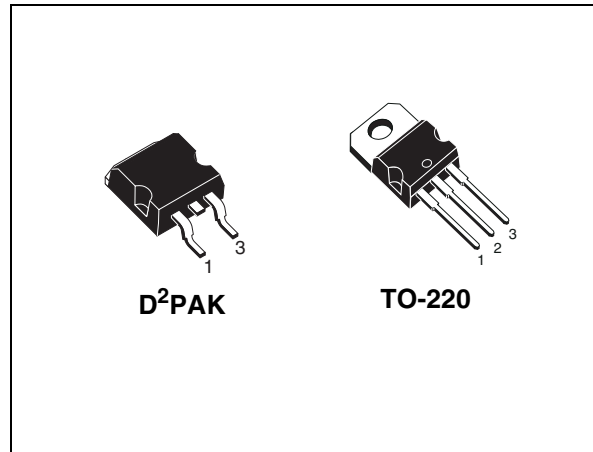


Figure 1. Internal schematic diagram

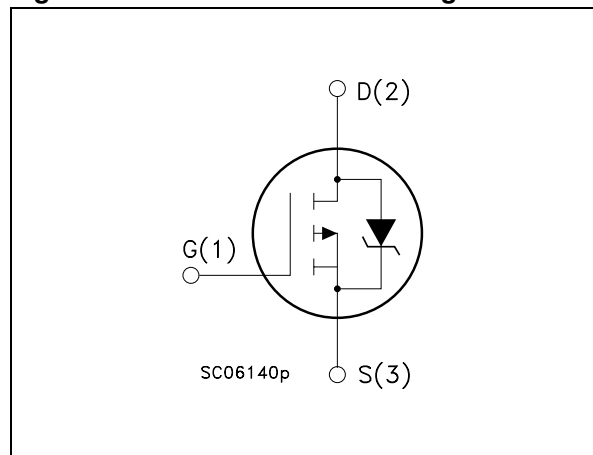


Table 1. Device summary

Order code	Marking	Package	Packaging
STP80PF55	P80PF55	TO-220	Tube
STB80PF55	B80PF55	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	55	V
V_{GS}	Gate-source voltage	± 16	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	57	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
	Derating factor	2	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	7	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.4	J
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Current limited by package.
2. Pulse width limited by safe operating area .
3. $I_{SD} \leq 40\text{A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD}=80\% V_{(BR)DSS}$.
4. Starting $T_j=25^\circ\text{C}$, $I_D=80\text{A}$, $V_{DD}=40\text{V}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ mA}$, $V_{GS} = 0$	55			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C=125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$		0.016	0.018	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $I_D = 40\text{ A}$	-	32		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	5500 1130 600		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$I_D = 25\text{ A}$, $V_{DD} = 80\text{ V}$, $V_{GS} = 10\text{ V}$ (see Figure 15)	-	190 27 65	258	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=25\text{ V}$, $I_D=40\text{ A}$, $R_G=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$ (see Figure 14)	-	35 190	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=25\text{ V}$, $I_D=40\text{ A}$, $R_G=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$ (see Figure 14)	-	165 80	-	ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	$V_{clamp}=40\text{ V}$, $I_D=80\text{ A}$, $R_G=4.7\text{ }\Omega$, $V_{GS}=10\text{ V}$ (see Figure 14)	-	60 40 85	-	ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 25\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	110		ns
Q_{rr}	Reverse recovery charge			495		μC
I_{RRM}	Reverse recovery current			9		A

1. Pulse width limited by T_{jmax} .

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5 %.

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 and D²PAK

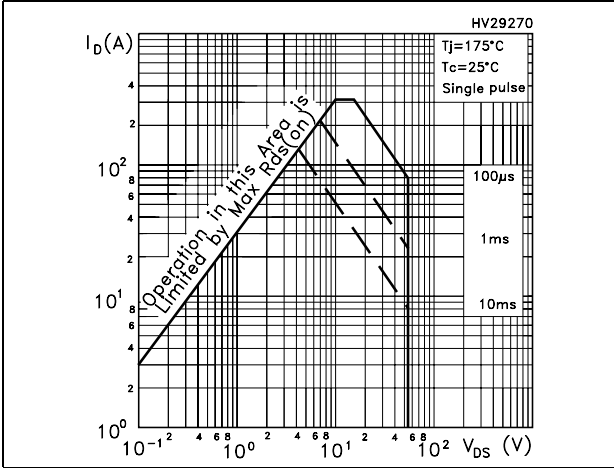


Figure 3. Thermal impedance for TO-220 and D²PAK

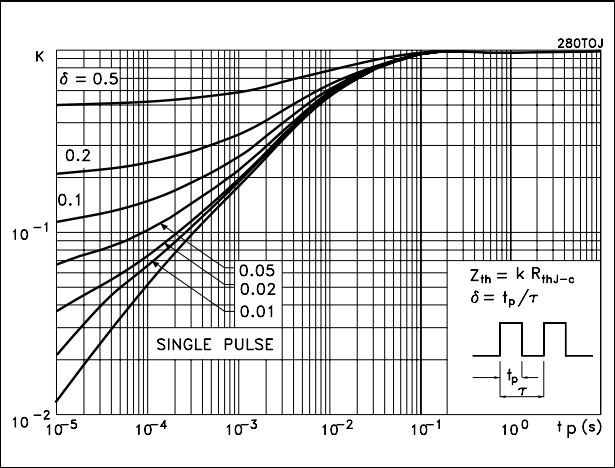


Figure 4. Output characteristics

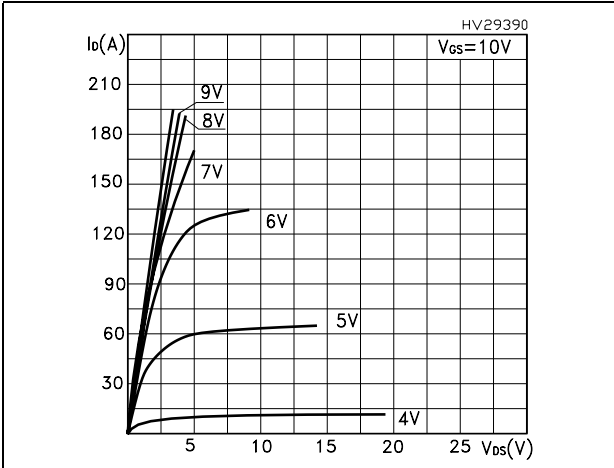


Figure 5. Transfer characteristics

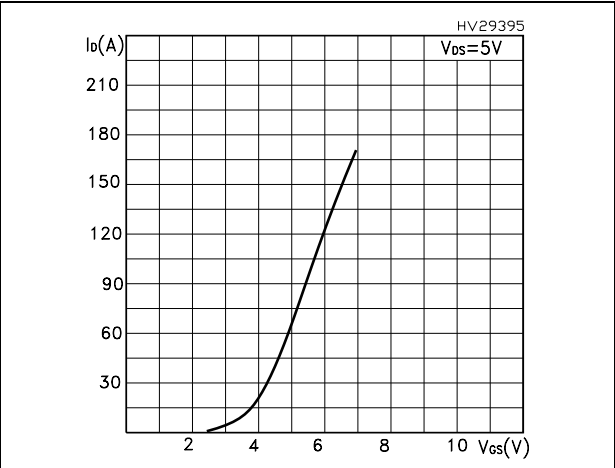


Figure 6. Transconductance

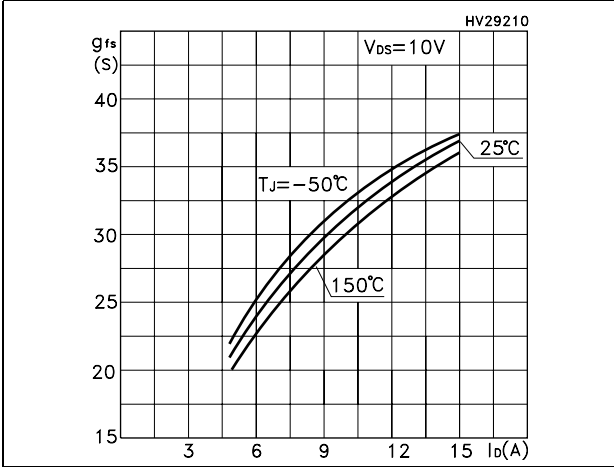


Figure 7. Static drain-source on resistance

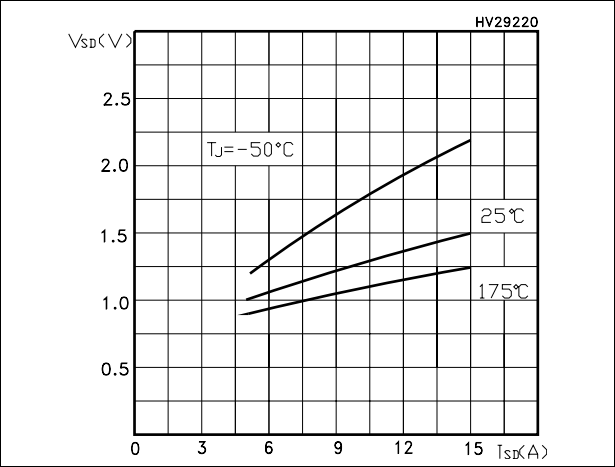


Figure 8. Gate charge vs gate-source voltage

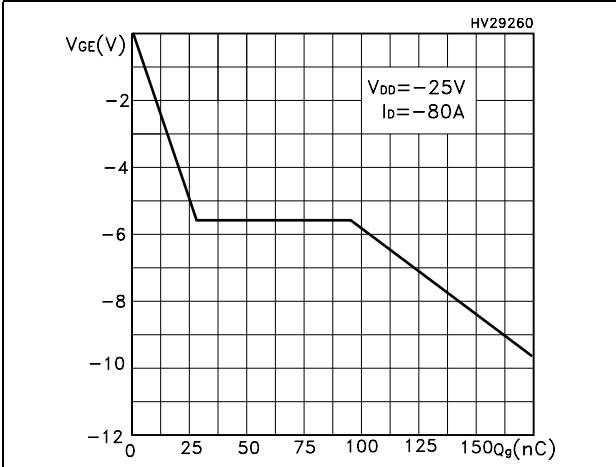


Figure 9. Capacitance variations

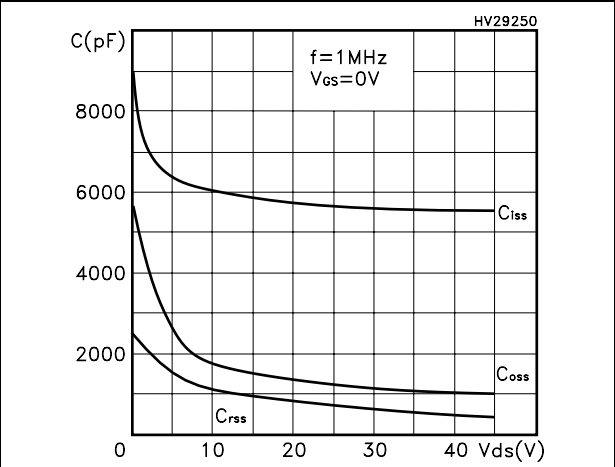


Figure 10. Normalized gate threshold voltage vs temperature

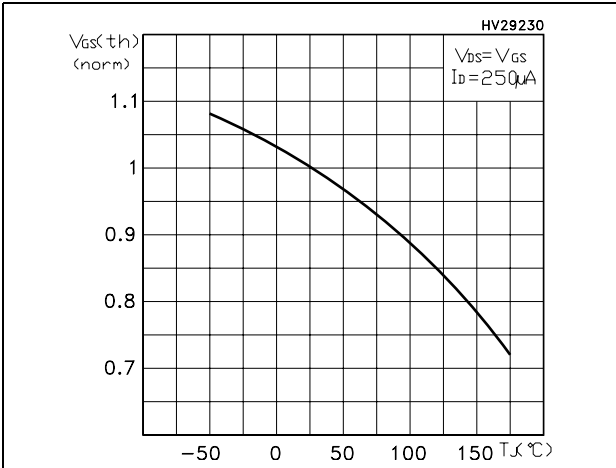


Figure 11. Normalized on resistance vs temperature

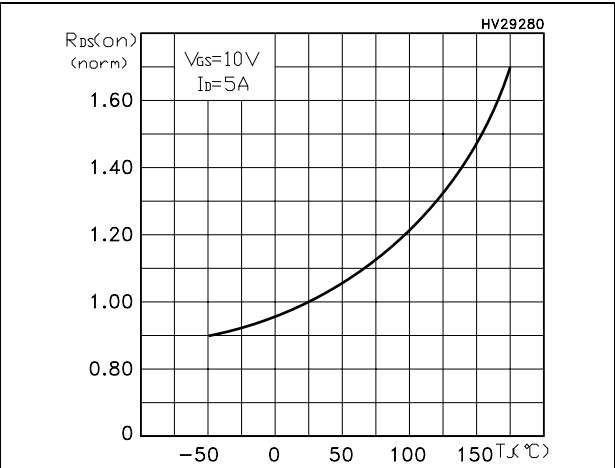


Figure 12. Source-drain diode forward characteristics

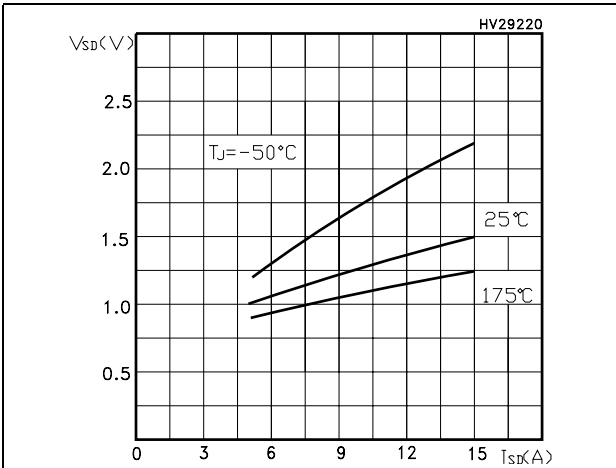
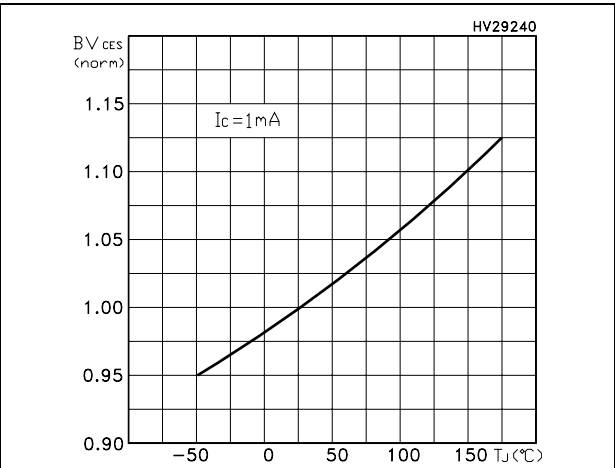


Figure 13. Normalized BV_{DSS} vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

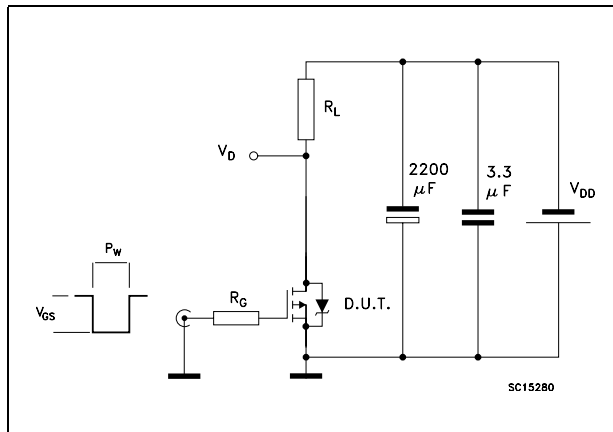


Figure 15. Gate charge test circuit

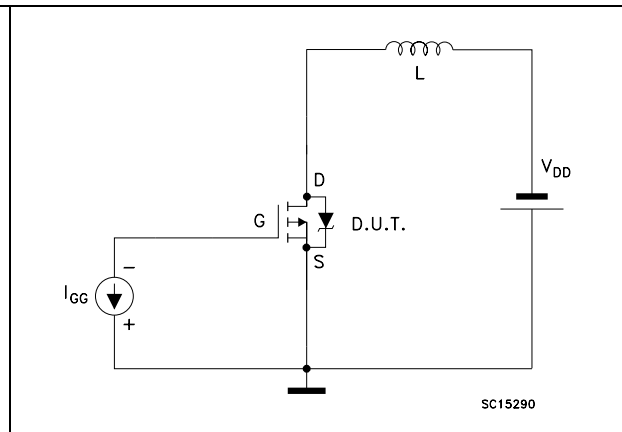
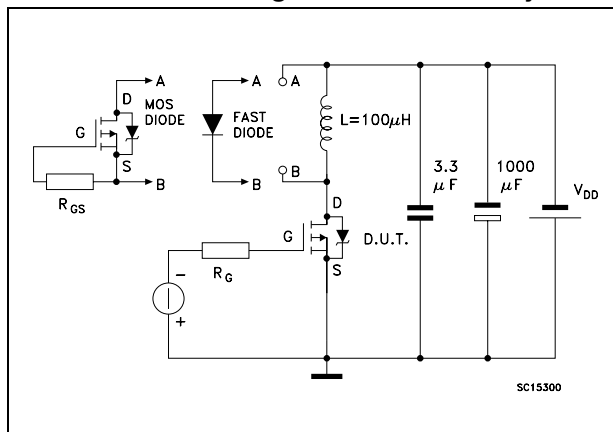


Figure 16. Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. D²PAK mechanical data

Dim	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°

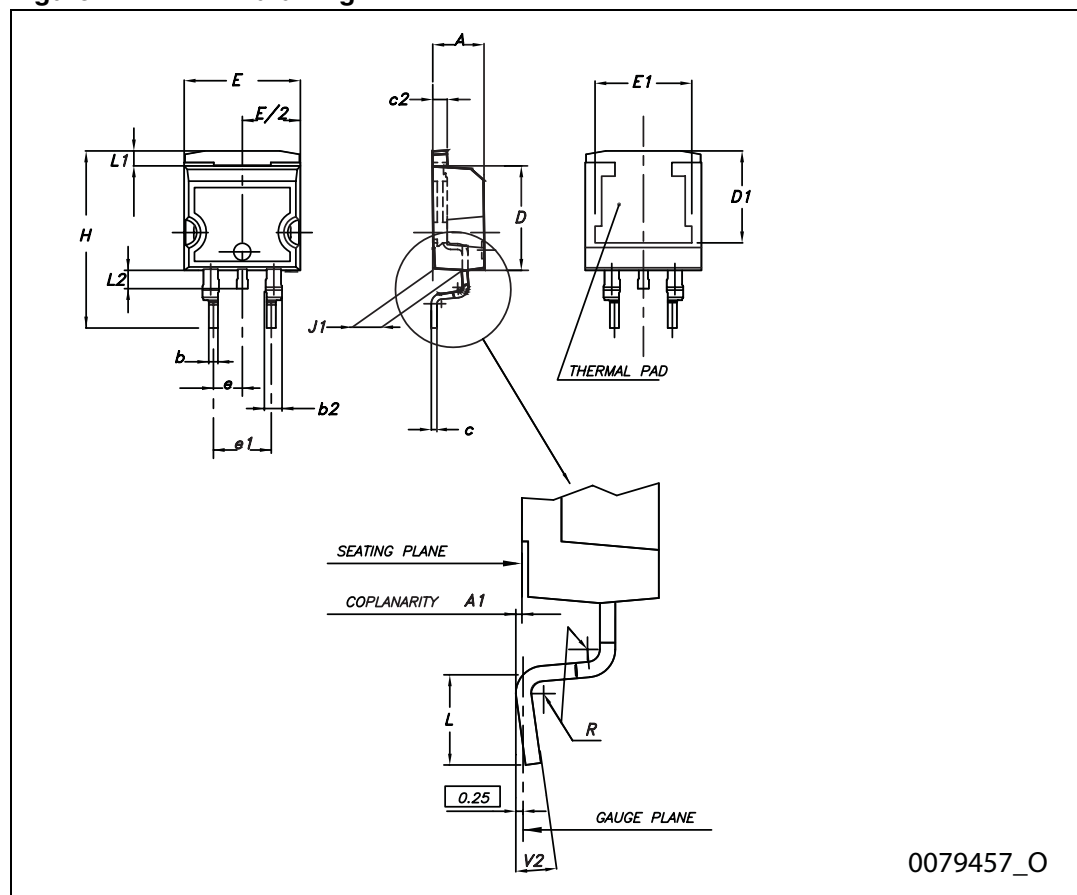
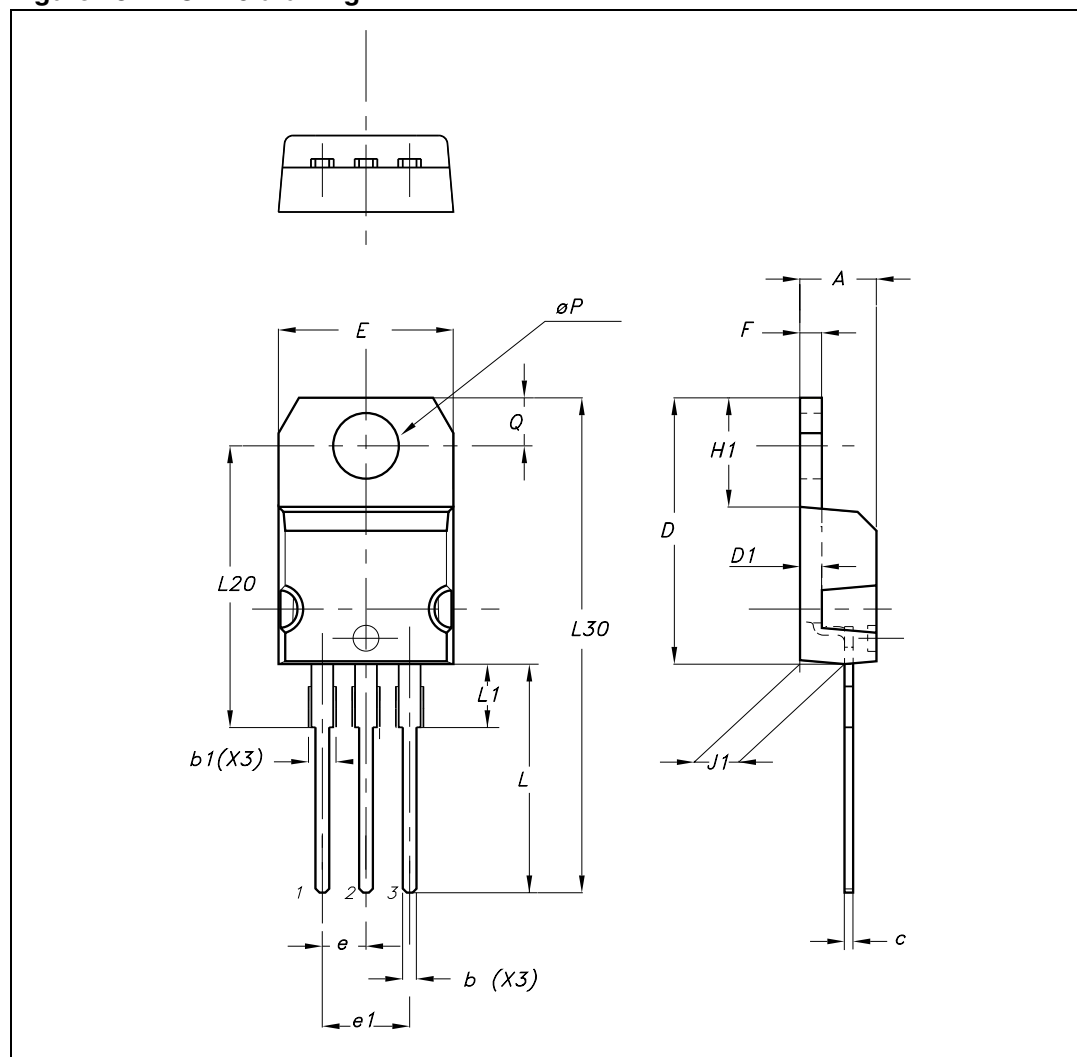
Figure 17. D²PAK drawing

Table 9. TO-220 mechanical data

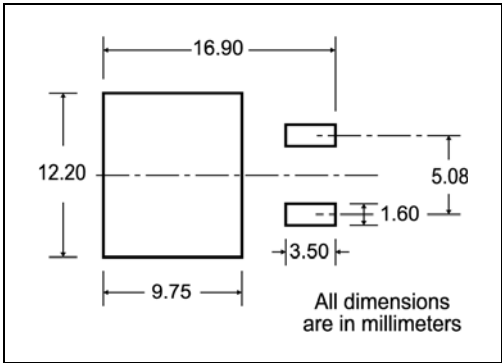
Dim	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 18. TO-220 drawing

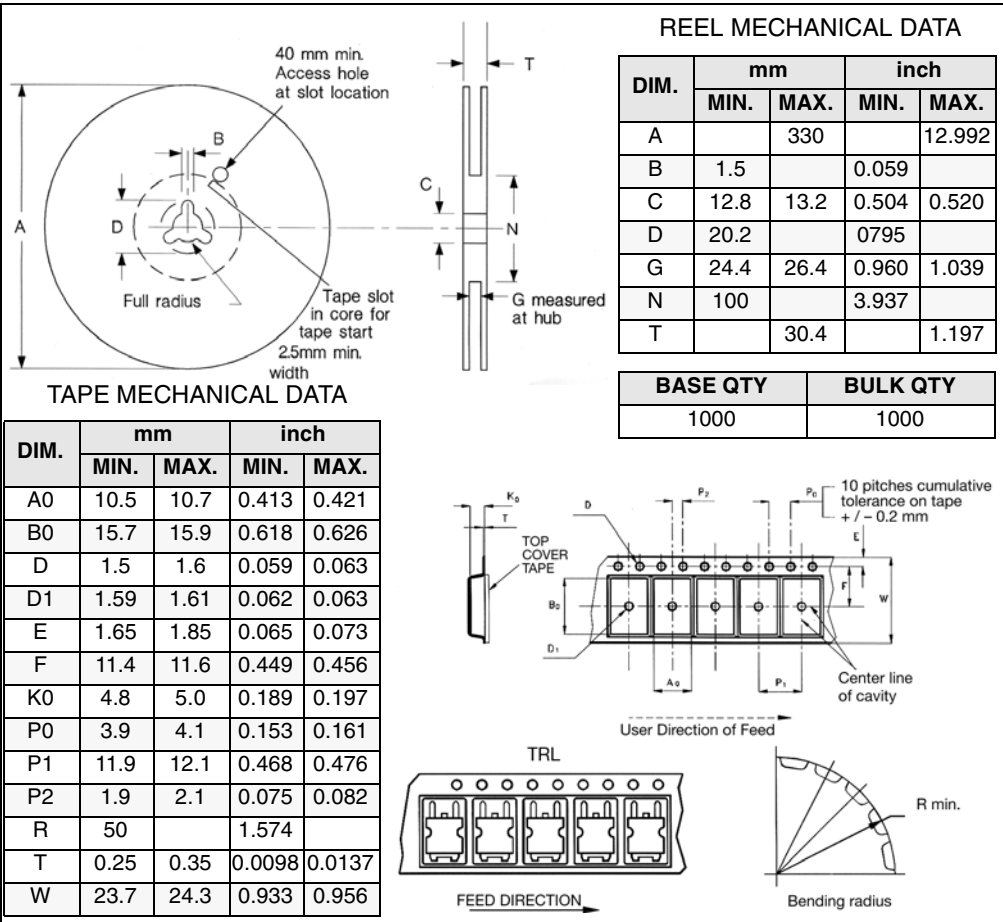


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
09-Sep-2004	4	Revalidation
12-Sep-2006	5	New template, D ² PAK added
09-Aug-2010	6	Content reworked to improve readability, no technical changes.

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