

SIPMOS[®] Small-Signal-Transistor

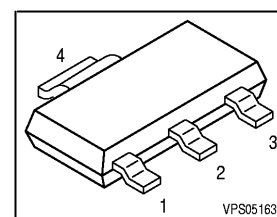
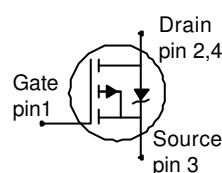
Feature

- P-Channel
- Enhancement mode
- Avalanche rated
- dv/dt rated
- Ideal for fast switching buck converter
- Pb-free lead plating; RoHS compliant
- Qualified according to AEC Q101
- Halogen-free according to IEC 61249-2-21

Product Summary

V_{DS}	-60	V
$R_{DS(on)}$	0.13	Ω
I_D	-2.9	A

PG-SOT223



Halogen-Free



Type	Package	Tape and reel	Packaging	Marking
BSP613P	PG-SOT223	H6327: 1000pcs/r.	Non Dry	BSP613P

Maximum Ratings, at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current	I_D	-2.9	A
$T_A = 25^{\circ}\text{C}$			
$T_A = 70^{\circ}\text{C}$		-2.3	
Pulsed drain current	$I_{D\text{ puls}}$	-11.6	
$T_A = 25^{\circ}\text{C}$			
Avalanche energy, single pulse	E_{AS}	150	mJ
$I_D = 2.9\text{ A}$, $V_{DD} = -25\text{ V}$, $R_{GS} = 25\Omega$			
Avalanche energy, periodic limited by T_{jmax}	E_{AR}	0.18	
Reverse diode dv/dt	dv/dt	6	kV/ μs
$I_S = 2.9\text{ A}$, $V_{DS} = -48\text{ V}$, $di/dt = -200\text{ A}/\mu\text{s}$, $T_{jmax} = 150^{\circ}\text{C}$			
Gate source voltage	V_{GS}	± 20	V
Power dissipation	P_{tot}	1.8	W
$T_A = 25^{\circ}\text{C}$			
Operating and storage temperature	T_j , T_{stg}	-55... +150	$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1		55/150/56	
ESD Class		Class 1c	
JESD22-A114-HBM			

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - soldering point (Pin 4)	R_{thJS}	-	-	19	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	100	-	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	100	
@ 6 cm ² cooling area ¹⁾		-	-	70	

Electrical Characteristics, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage $V_{GS}=0, I_D=-250\mu A$	$V_{(BR)DSS}$	-60	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D=-1mA$	$V_{GS(th)}$	-2.1	-3	-4	
Zero gate voltage drain current $V_{DS}=-60V, V_{GS}=0, T_j=25^{\circ}C$ $V_{DS}=-60V, V_{GS}=0, T_j=125^{\circ}C$	I_{DSS}	-	-0.1 -10	-1 -100	μA
Gate-source leakage current $V_{GS}=-20V, V_{DS}=0$	I_{GSS}	-	-10	-100	
Drain-source on-state resistance $V_{GS}=-10V, I_D=2.9A$	$R_{DS(on)}$	-	0.11	0.13	Ω

¹⁾ Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics, at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic Characteristics

Transconductance	g_{fs}	$ V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$, $I_D = 2.9\text{A}$	2.7	5.4	-	S
Input capacitance	C_{iss}	$V_{GS} = 0$, $V_{DS} = -25\text{V}$, $f = 1\text{MHz}$	-	715	875	pF
Output capacitance	C_{oss}		-	230	295	
Reverse transfer capacitance	C_{rss}		-	90	120	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -30\text{V}$, $V_{GS} = -10\text{V}$, $I_D = 2.9\text{A}$, $R_G = 2.7\Omega$	-	6.7	17	ns
Rise time	t_r		-	9	18	
Turn-off delay time	$t_{d(off)}$		-	26	52	
Fall time	t_f		-	7	19	

Gate Charge Characteristics

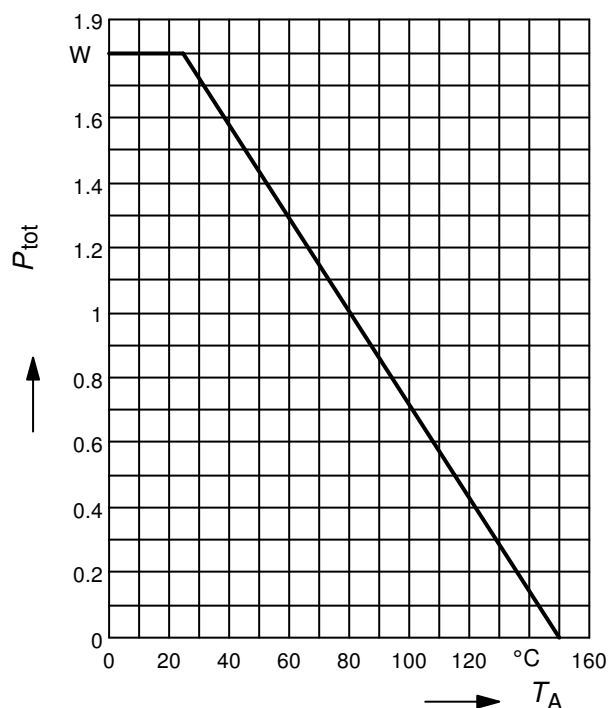
Gate to source charge	Q_{gs}	$V_{DD} = -48\text{V}$, $I_D = 2.9\text{A}$	-	2.5	3.8	nC
Gate to drain charge	Q_{gd}		-	8.9	14.3	
Gate charge total	Q_g	$V_{DD} = -48\text{V}$, $I_D = 2.9\text{A}$, $V_{GS} = 0$ to -10V	-	22	33	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = -48\text{V}$, $I_D = 2.9\text{A}$	-	-3.9	-	V

Reverse Diode

Inverse diode continuous forward current	I_S	$T_A = 25^{\circ}\text{C}$	-	-	-2.9	A
Inv. diode direct current, pulsed	I_{SM}		-	-	-11.6	
Inverse diode forward voltage	V_{SD}	$V_{GS} = 0\text{V}$, $ I_F = I_S $	-	-0.8	-1.1	V
Reverse recovery time	t_{rr}	$V_R = -30\text{V}$, $ I_F = I_S $, $di_F/dt = 100\text{A}/\mu\text{s}$	-	37.2	79	ns
Reverse recovery charge	Q_{rr}		-	59.8	112	nC

1 Power Dissipation

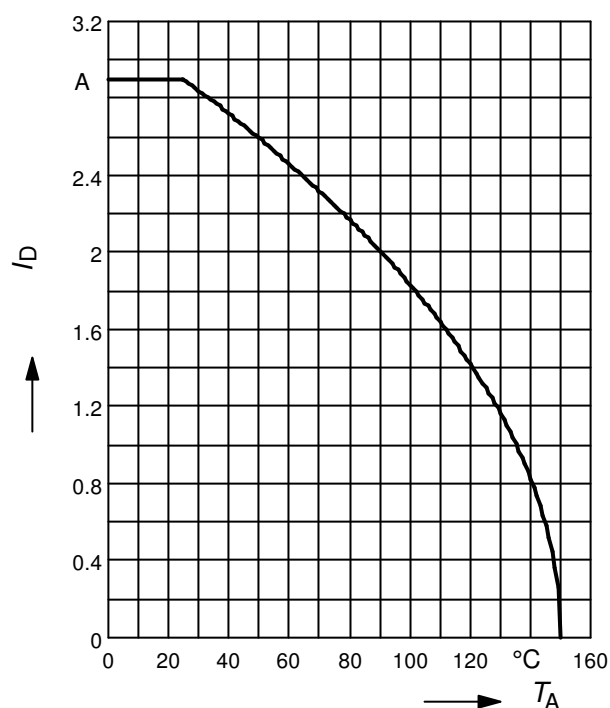
$$P_{\text{tot}} = f(T_A)$$



2 Drain current

$$I_D = f(T_A)$$

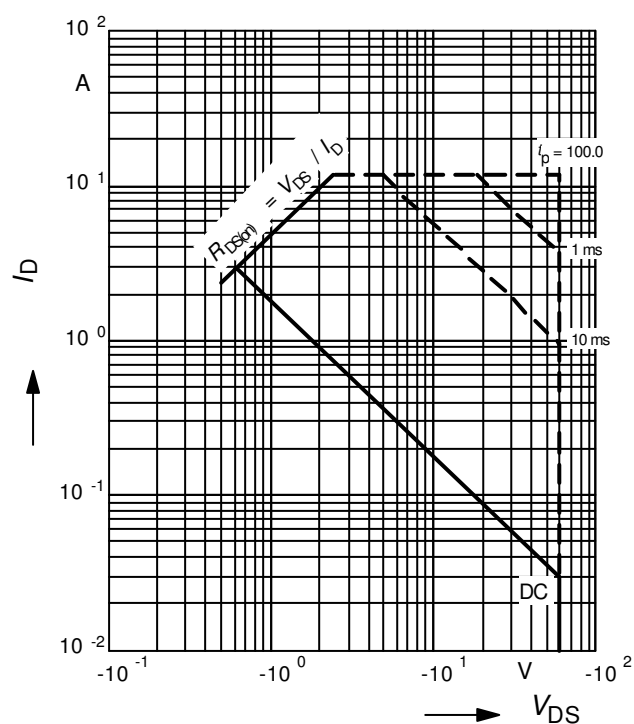
parameter: $V_{GS} \geq 10 \text{ V}$



3 Safe operating area

$$I_D = f(V_{DS})$$

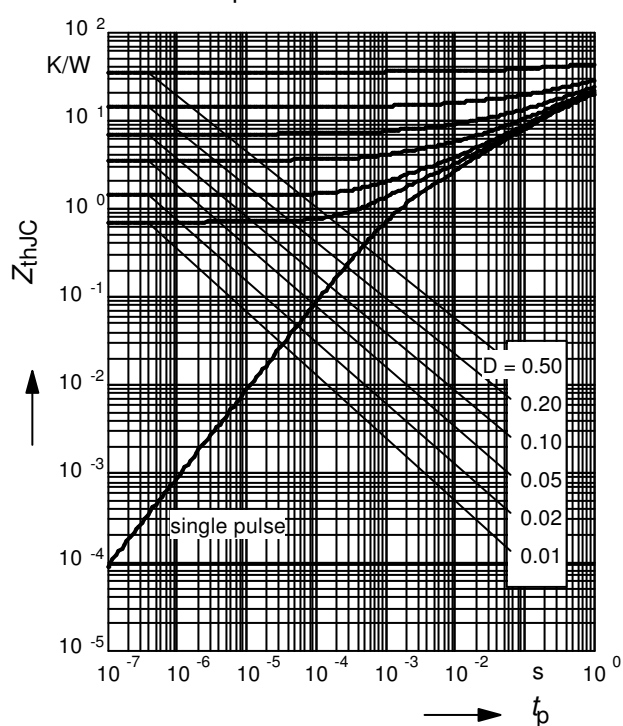
parameter: $D = 0$, $T_A = 25 \text{ °C}$



4 Transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

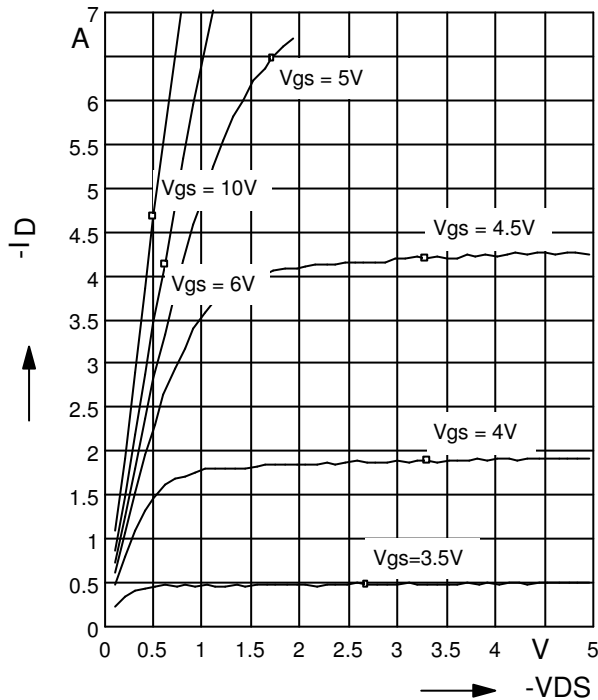
parameter: $D = t_p / T$



5 Typ. output characteristic

$$I_D = f(V_{DS})$$

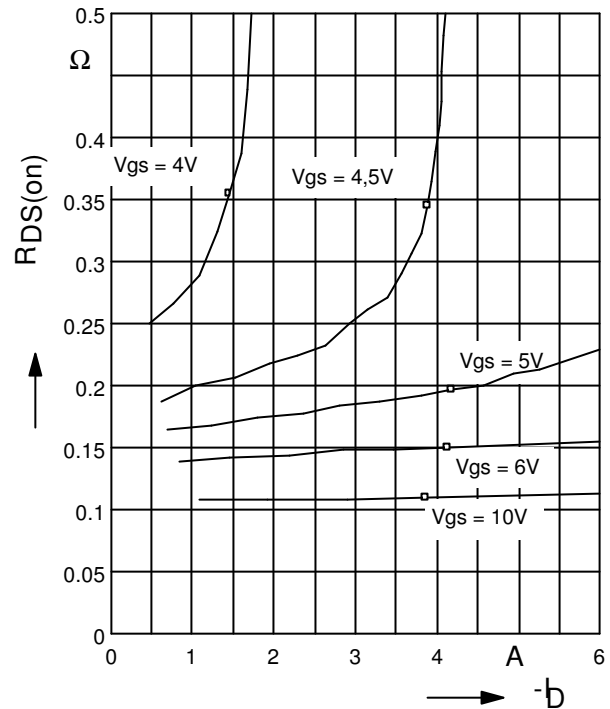
parameter: $T_j = 25^\circ\text{C}$



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D)$$

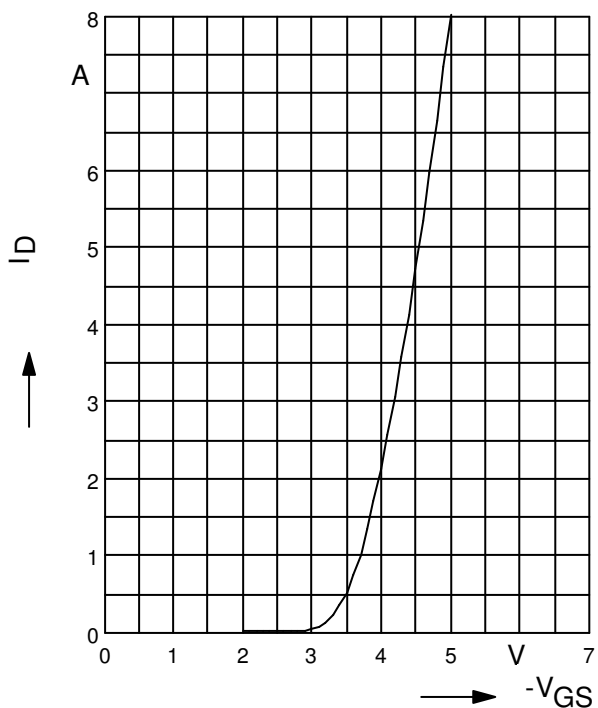
parameter: V_{GS} ; $T_j = 25^\circ\text{C}$



7 Typ. transfer characteristics

$$I_D = f(V_{GS}); |V_{DS}| \geq 2 \times |I_D| \times R_{DS(on)max}$$

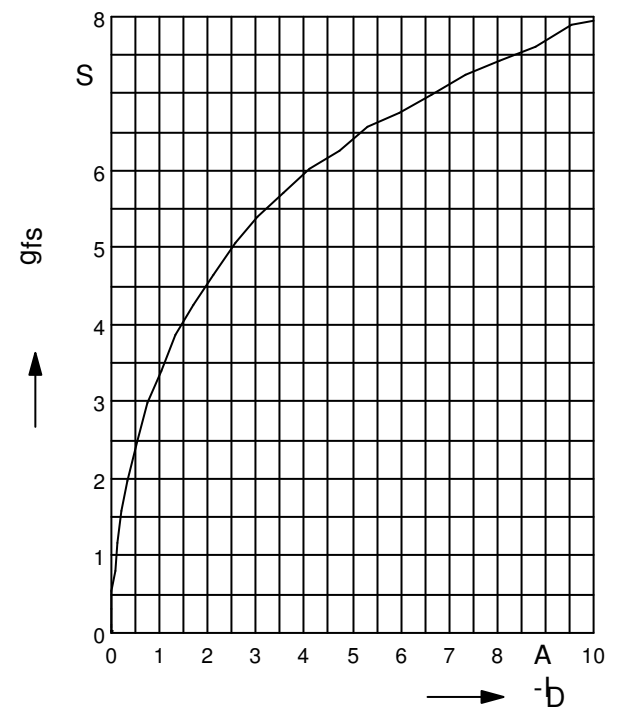
parameter: $T_j = 25^\circ\text{C}$



8 Typ. forward transconductance

$$g_{fs} = f(I_D)$$

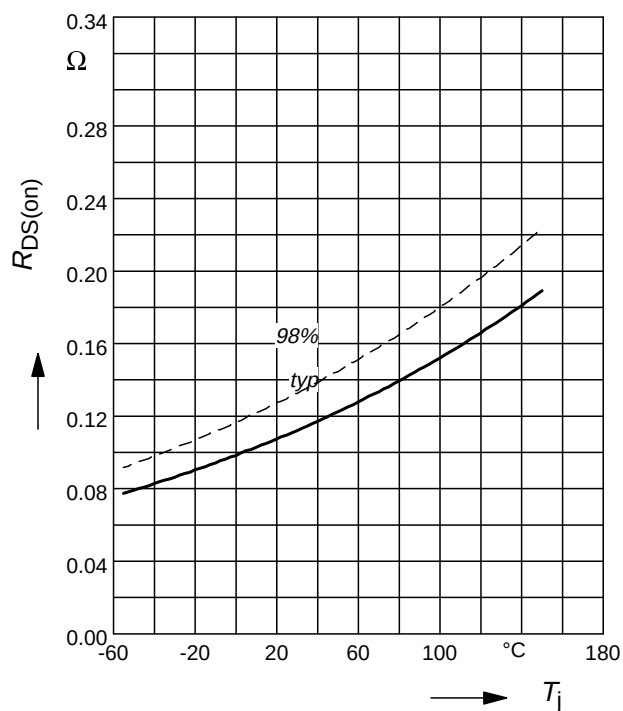
parameter: $T_j = 25^\circ\text{C}$



9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

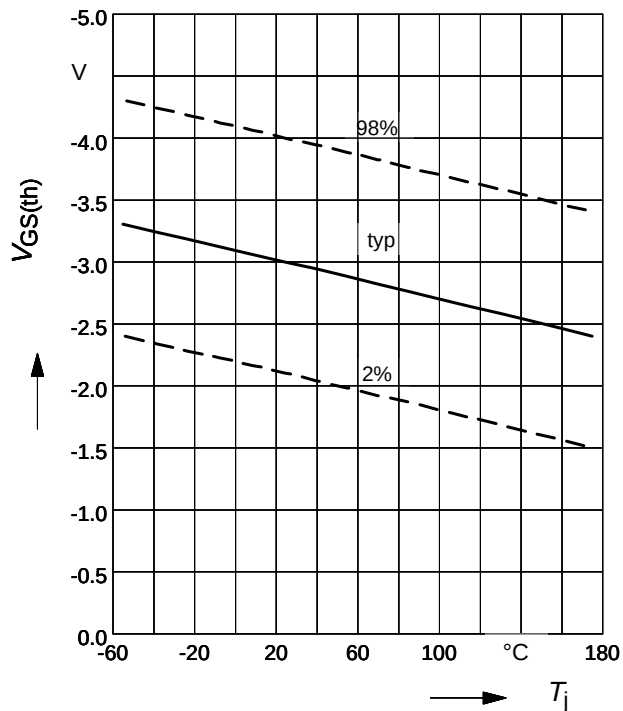
parameter : $I_D = -2.9 \text{ A}$, $V_{GS} = -10 \text{ V}$



10 Gate threshold voltage

$$V_{GS(th)} = f(T_j)$$

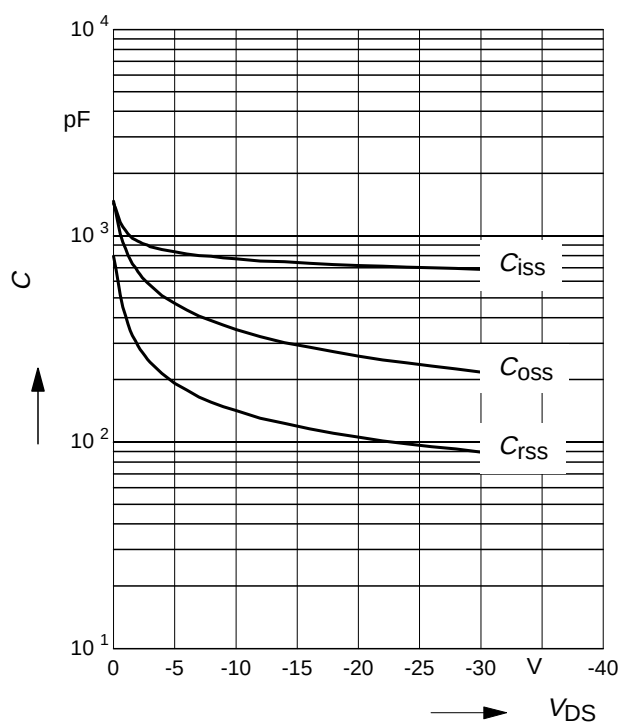
parameter: $V_{GS} = V_{DS}$, $I_D = -1 \text{ mA}$



11 Typ. capacitances

$$C = f(V_{DS})$$

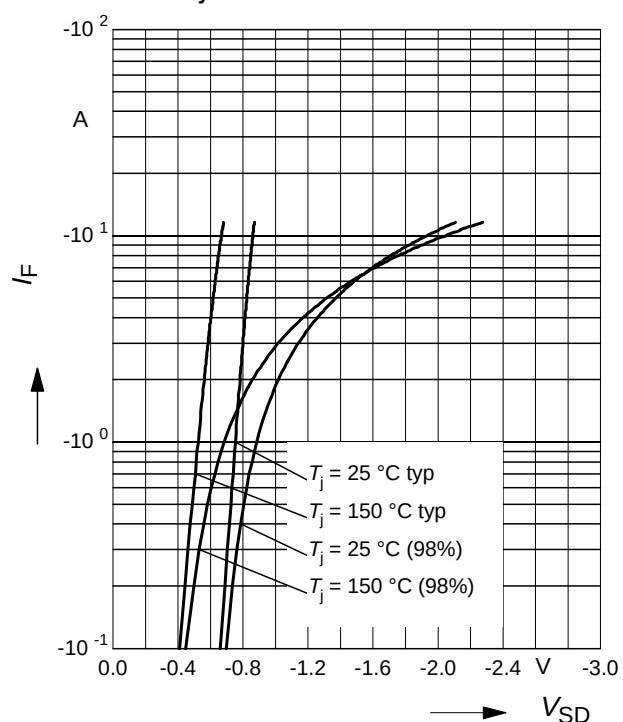
parameter: $V_{GS}=0\text{V}$, $f=1 \text{ MHz}$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

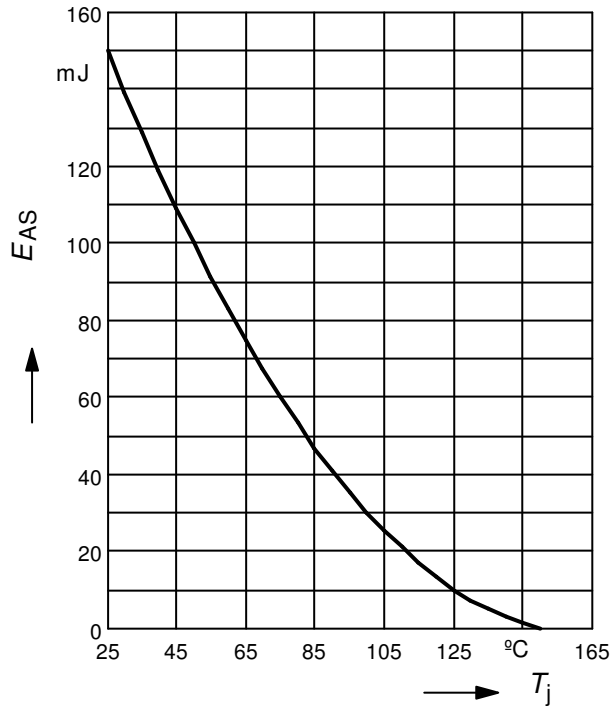
parameter: T_j , $t_p = 80 \mu\text{s}$



13 Typ. avalanche energy

$$E_{AS} = f(T_j)$$

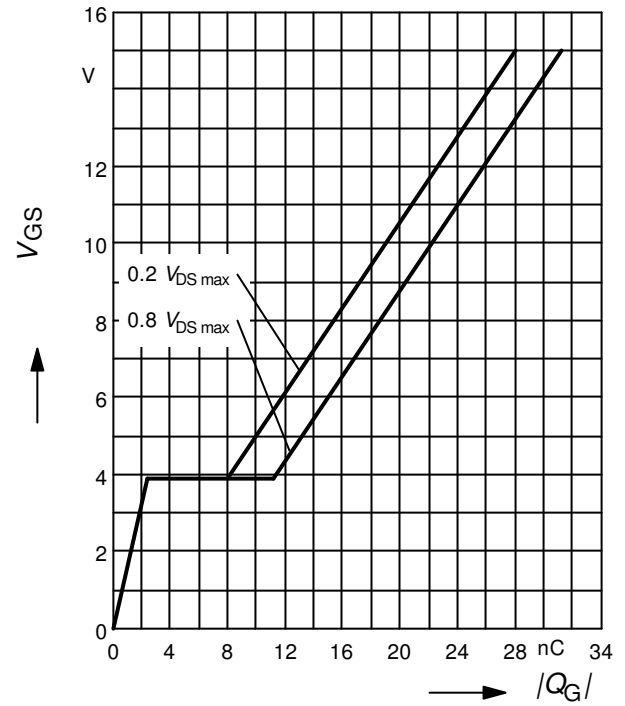
par.: $I_D = 2.9 \text{ A}$, $V_{DD} = -25 \text{ V}$, $R_{GS} = 25 \Omega$



14 Typ. gate charge

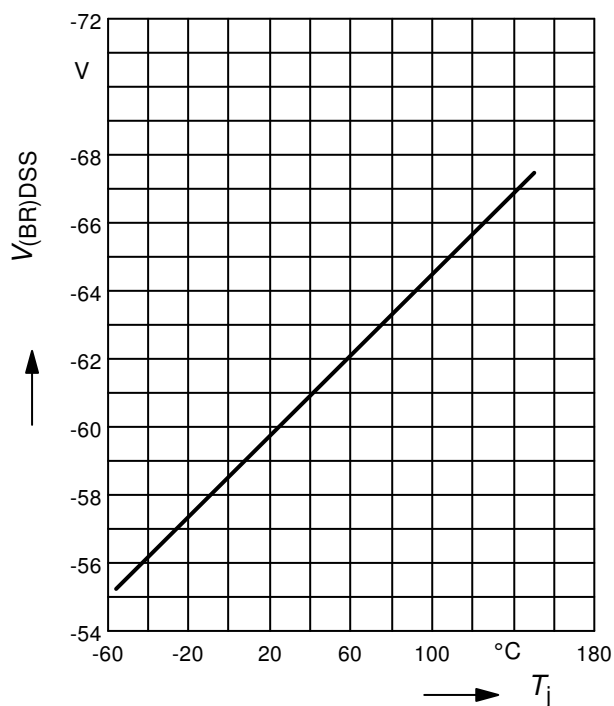
$$V_{GS} = f(Q_G), \text{ parameter: } V_{DS}; T_j = 25 \text{ °C}$$

$I_D = 2.9 \text{ A}$ pulsed;

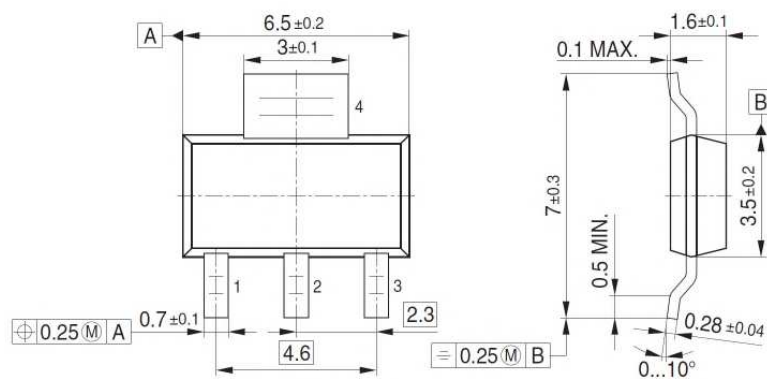


15 Drain-source breakdown voltage

$$V_{(BR)DSS} = f(T_j)$$

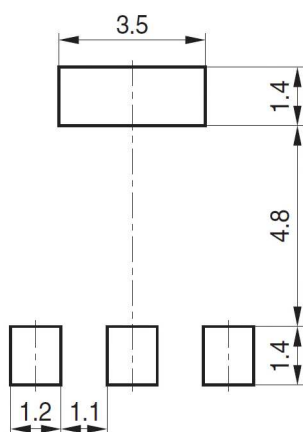


Package Outline SOT-223

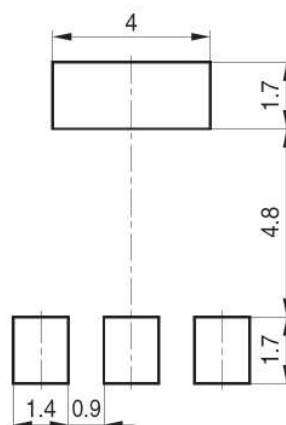


Footprint

Soldering type: Reflow soldering



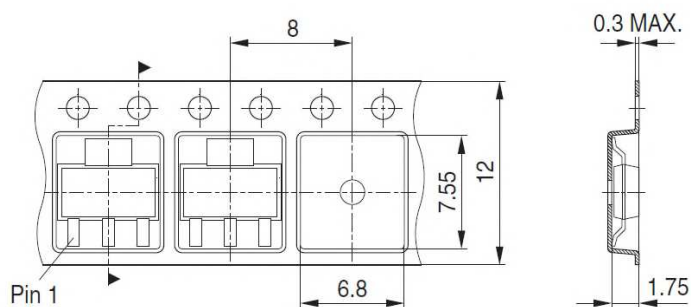
Soldering type: Wave soldering



Tape and Reel

Reel ø180 mm: 1.000 Pieces/Reel
Reels/Box: 1 x 1.000 = 1.000

Reel ø330 mm: 4.000 Pieces/Reel
Reels/Box: 1 x 4.000 = 4.000



Dimensions in mm

Revision History

BSP613P

Revision: 2016-06-13, Rev. 2.8

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.8	2016-06-13	Insert package outlines

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